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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,937	06/24/2003	Nicholas A. Oleksinski	03-0228	1794

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/602,937	OLEKSINSKI ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to the response filed on 01/21/05. The applicant argument regarding Batchelor Dennis is not persuasive; therefore, all the rejections based on Batchelor Dennis is retained and repeated for the following reasons.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Batchelor Dennis (U.S Patent 2004/0025129).

4. As to claims 1, 14, 20 and 21 Batchelor teaches a method for generating a plurality of timing constraints for a circuit design, comprising the steps of: (A) identifying a plurality of clock signals by analyzing said circuit design (see fig 4, fig 6 element 475 paragraph 0061); (B) determining a plurality of relationships among said clock signals (see fig1-4 and fig 6 paragraph 0026-0029 Batchelor teaches a relative timing between clock paragraph 0059 and paragraph 0061 Batchelor teaches timing analyzer 465 may be programmed with a constraint generator 610 and constraint generator 610 receives relative timing information for signal interfaces as described above with regard to the representative circuit 300 as described Fig 3); and generating said timing constraints for said circuit design in response to said clock signals and said relationships (see fig 6 elemnet 465 and 610 and paragraph 0059 to paragraph 0063).

5. As to claim 2, Batchelor teaches wherein said plurality of clock signals comprises a test clock signal (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

6. As to claim 3, and Batchelor teaches further comprising the step of: eliminating from said timing constraints each signal connected to an internal mode pin for said circuit design that defines a non-clock signal (see fig 6 element 465 paragraph 0060 and parapraph 0061).

7. As to claim 4, Batchelor teaches further comprising the step of: eliminating from said timing constraints each signal connected to an external interface for said circuit design that defines a non-clock signal (see fig 6 element 465 paragraph 0060 and parapraph 0061).

8. As to claim 5, Batchelor teach wherein step (C) is in further response to a plurality of parameters associated with said clock signals (see paraphraph 0016 and parapraph 0064).

9. As to claim 6, Batchelor teaches wherein at least one of said parameters relates to a test clock signals of said clock signals (see paraphraph 0016 and parapraph 0064).

10. As to claim 7, Batchelor teaches further comprising the step eliminating from said timing constraints each signal for said circuit design that defines a static signal (fig 1-5 col 2 lines 23-61 and col 3 lines 16 to col 4 lines 64).

11. As to claim 8, Batchelor teaches wherein step (B) comprises the sub-step of: generating an asynchronous relationship of said relationships between at least two of said clock signals operating asynchronously to each other (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

12. As to claim 9, Batchelor teach wherein step (B) comprises the sub-step of: generating a fastest clock relationship of said relationships between at least two of said clock signals operating at different speeds between two clock boundaries of said circuit design (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

13. As to claim 10, Batchelor teaches wherein step (B) comprises the sub-step of: generating a multiplexed clock relationship of said relationships between at least two of said clock signals routable through a multiplexer in said circuit design (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

14. As to claim 11, Batchelor teaches wherein step (B) comprises the sub-step of: generating a derivative clock relationship of said relationships between a first of said clock signals that is derived from a second of said clock signals (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

15. As to claim 12, Batchelor teaches wherein step (B) comprises the sub-step of: generating a shared structure relationship of said relationships between a test clock signal of said clock signals and a normal clock signal particular structure of said circuit design in different modes for said circuit design (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

16. As to claim 13, Batchelor teach further comprising the step of: writing said timing constraints among a plurality of files (see paragraph 0016 and paragraph 0064).

17. As to claim 15, Batchelor teaches further comprising determining a plurality of relationships among said clock signals, wherein said timing constraints are generated in further response said relationships (see fig 4 and fig 6 paragraph 0059 and paragraph 0061).

18. As to claim 16, Batchelor teaches wherein step (B) comprises the sub-step of: querying said user for a frequency parameter of said parameters f or each of said clock signals (see paragraph 0016 and paragraph 0064).

19. As to claim 17, Batchelor teaches wherein step (B) comprises the sub-step of: querying said user for a timing uncertainty parameter of said parameters for each of said clock signals (see paragraph 0016 and paragraph 0064).

20. As to claim 18, Batchelor teaches wherein said circuit design comprises a gate level design (see paragraph 0016 and paragraph 0064 and background).

21. As to claim 19, Batchelor teach wherein said circuit design comprises a register transfer language design (see paragraph 0016 and paragraph 0064 and background).

Response to Amendment and Arguments

22. Applicant's arguments filed January 21, 2005 have been fully considered but they are not persuasive.

Applicant contends that Dennis Batchelor does not describle "a plurality of relationships among a plurality of clock signals by analyzing said circuit design" as claimed. In response to Applicant's argument that Dennis Batchelor does not describle "a plurality of relationships among a plurality of clock signals by analyzing said circuit design" as claimed, Examiner respectfully disagrees. Applicant is directed to (see fig1-4 and fig 6 paragraph 0026-0029 Batchelor teaches a relative timing between clock and paragraph 0059 and paragraph 0061 Batchelor teaches timing analyzer 465 may be programmed with a constraint generator 610 and constraint generator 610 receives relative timing information for signal interfaces as described above with regard to the representative circuit 300 as described Fig 3). For this reason, examiner holds the rejection proper.

23. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within -1W0 MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1908. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
April 16, 2005

VUTHE SIEK
PRIMARY EXAMINER